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A Novel Integrated AC-DC Five Level Converter Strategy for Power Factor Correction

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ABSTRACT

Multilevel configuration has the advantage of its simplicity and modularity over the configurations of the other converters. With the application of multilevel converter in the high voltage and large power occasions in recent years, its modulation strategy has become a research hot point in the field of power electronics. The proposed power-factor-correction circuit can achieve unity power factor and ripple-free input current using a coupled inductor. The proposed rectifier can also produce input currents that do not have dead band regions and an output current that is continuous for all load conditions. The features of this converter are that it has lower input section peak current stresses and a better harmonic content than similar converter with a non-interleaved output, the output current is continuous for all load ranges, and the dc bus voltage is less than 450 for all line and load conditions. In this paper, the operation of the new converter is explained, its steady-state characteristics are determined by analysis, and these characteristics are used to develop a procedure for the design of the converter. Hence the simulation results are obtained using MATLAB/SIMULINK software. The proposed system provides a closed loop control for variable output voltage. The SSPFC AC/DC converter can operate with lower peak voltage stresses across the switches and the DC bus capacitors as it is a three-level converter. The proposed concept can be implemented with 5-level for efficient output voltage.

Keywords -*Power Factor Correction (PFC), Single –Stage, Five Level Topology, Total Harmonic Distortion (THD).*

I. INTRODUCTION

Electric Power quality is a term which has captured increasing attention in power engineering in the recent years. Even though this subject has always been of interest to power engineers; it has assumed considerable interest in the 1990's. Electric power quality means different things for different people. To most electric power engineers, the term refers to a certain sufficiently high grade of electric service but beyond that there is no universal agreement. The goal of developing AC/DC converters with Isolation and Power Factor Correction (PFC) feature in a single power processing stage and without a mandatory full-bridge rectifier has for years eluded power electronics researchers. Present AC/DC converters operated from a single-phase AC line are based on conventional Pulse Width Modulation (PWM) switching and process the power through at least three distinct power processing stages: full-bridge rectifier followed by boost PFC converter and another cascaded isolated full-bridge DC/DC

converter stage, which together use a total of 14 switches and three magnetic components resulting in corresponding efficiency, size and cost limitations. Power-electronic inverters are becoming popular for various industrial drives applications. In recent years also high-power and medium-voltage drive applications have been installed. To overcome the limited semiconductor voltage and current ratings, some kind of series and/or parallel connection will be necessary. Due to their ability to synthesize waveforms with a better harmonic spectrum and attain higher voltages, multi-level inverters are receiving increasing attention in the past few years.

Another method is using an ac–dc boost converter in the front-end rectifying stage to perform active PFC for most applications. The ac–dc boost converter shapes the input line current as an almost sinusoidal shape with a harmonic content compliant with agency standards. Using active PFC, however, increases the cost and complexity of the overall two-stage converter because an additional switching converter must be implemented [2]. This has led to the emergence of single-stage power factor-corrected (SSPFC) converters.

There have been numerous publications about SSPFC converters, particularly for low-power ac–dc fly back and forward converters [1]–[11]. Research on the topic of higher power ac–dc single-stage full-bridge converters, however, has proved to be more challenging, and thus, there have been much fewer publications [12]–[14].Several single-stage ac–dc full-bridge current fed converters have been proposed [2]; these converters have a boost inductor connected to the input of the full bridge circuit. Although they can achieve a near-unity input power factor, they lack an energy-storage capacitor across the primary-side dc bus, which can result in the appearance of high voltage overshoots and ringing across the dc bus. It also causes the output voltage to have a large low-frequency 120-Hz ripple that limits their applications.

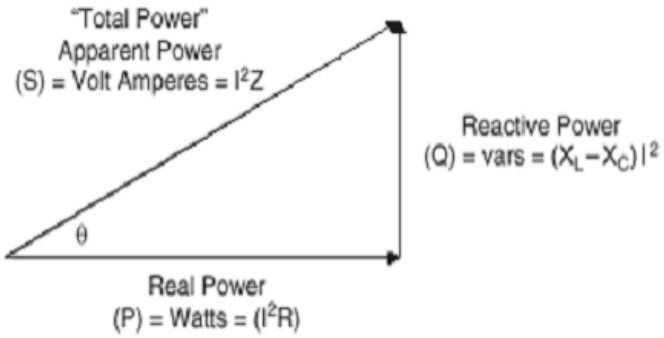

Fig.1 Power Factor Triangle

Power Factor Correction (PFC) technique continues to be attractive research topic with several effective regulations being reported. Conventional cascade of two stage topology can achieve good performance such as high power factor and low voltage stress, but it usually suffers from high cost and increased circuit complexity. Many single-stage PFC AC/DC converters have been proposed that can be applied cost-effectively. However, it's well known that in single stage topologies, the voltage across the bulk capacitor cannot be controlled well due to the fact that only one switch and control loop are used. Moreover, the storage capacitor voltage varies widely with the input voltage and load variation, especially.

II. MULTILEVEL INVERTER

The general structure of the multilevel inverter is to synthesize a sinusoidal voltage from several levels of voltages typically obtained from capacitor voltage sources. The so-called "multilevel" starts from three levels. A three level inverter, also known as a "neutral-clamped" inverter, consists of two capacitor voltages in series and uses the center tap as the neutral. Each phase leg of the three-level inverter has two pairs of switching devices in series. The center of each device pair is clamped to the neutral through clamping diodes. The output obtained from a three-level inverter is a quasi-square wave output if fundamental frequency switching is used. Multilevel inverters are being considered for an increasing number of applications due to their high power capability associated with lower output harmonics and lower commutation losses. Multilevel inverters have become an effective and practical solution for increasing power and reducing harmonics of AC load. The main multilevel topologies are classified into three categories: diode clamped inverters, flying capacitor inverters, and cascaded inverters. In a three-phase inverter system, the number of main switches of each topology is equal. Comparing with the number of other components, for example, clamping diodes and dc-link capacitors having the same capacity per unit, diode clamped inverters have the least number of capacitors among the three types but require additional clamping diodes. Flying capacitor inverters need the most number of capacitors. But cascaded inverters are considered as having the simplest structure.

The diode clamped inverter, particularly the three-level one, has drawn much interest in motor drive applications because it needs only one common voltage source. Also, simple and efficient PWM algorithms have been developed for it, even if it has inherent unbalanced dc-link capacitor voltage problem. However, it would be a limitation to applications beyond four-level diode clamped inverters for the reason of reliability and complexity considering dc-link balancing and the prohibitively high number of clamping diodes. Multilevel PWM has lower dv/dt than that experienced in some two-level PWM drives because switching is between several smaller voltage levels. Diode clamped multilevel inverter is a very general and widely used topology. DCMLI works on the concept of using diodes to limit voltage stress on power devices. A DCMLI typically consists of (m-1) capacitors on the DC bus where m is the total number of positive, negative and zero levels in the output voltage. Figure 2 shows a five level diode clamped inverter. The order of numbering of the switches for phase a is S1, S2, S3, S4, S5, S6, S7 and S8 and likewise for other two phases. The DC bus consists of four capacitors C1, C2, C3 and C4 acting as voltage divider. For a DC bus voltage Vdc, the voltage across each capacitor is Vdc/4 and voltage stress on each device is limited to Vdc/4 through clamping diode. The middle point of the four capacitors „n" can be defined as the neutral point. The principle of diode clamping to DC-link voltages can be extended to any number of voltage levels. Since the voltages across the semiconductor switches are limited by conduction of the diodes connected to the various DC levels, this class of multilevel inverter is termed diode clamped MLI. Table 1 shows the output voltage levels and the corresponding switch states for the chosen five level DCMLI. The switches are arranged into 4 pairs (S1, S5), (S2, S6), (S3, S7), (S4, S8). If one switch of the pair is turned on, the complementary switch of the same pair must be off. Four switches are triggered at any point of time to select the desired level in the five levels DCMLI.

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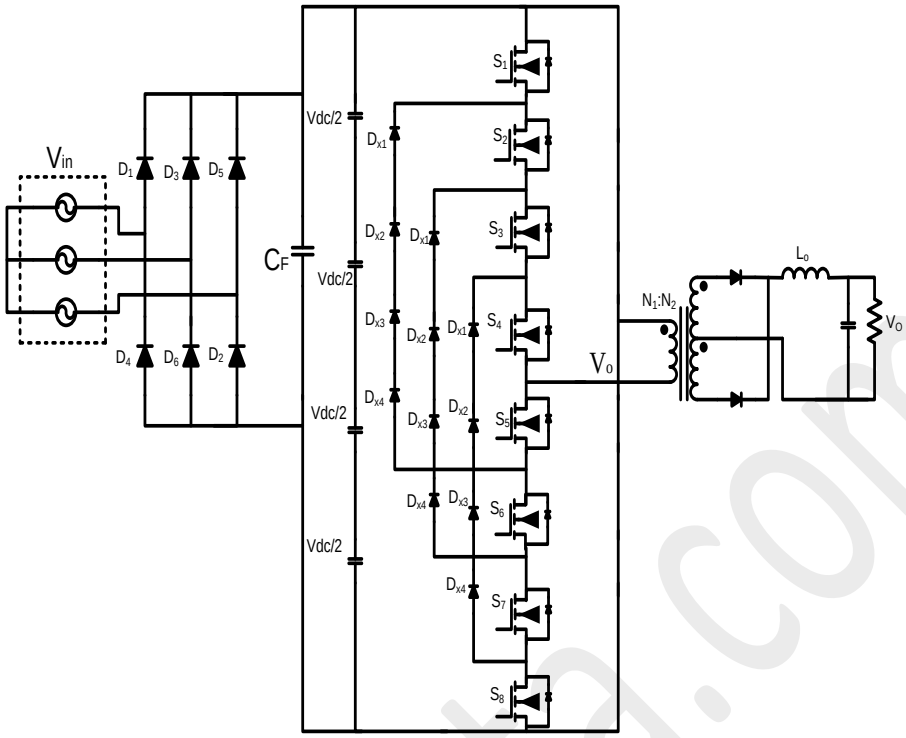

Fig.2. interleaved three-stage five level converters.

Mode1: output voltage of VO=0, two upper switches S3, S4 and two lower switches S5 and S6 are turned on.

Mode2: output voltage of VO=Vdc/4, three upper switches S2, S3, S4 and one lower switch S5 are turned on.

Mode3: output voltage of VO=Vdc/2, all upper switches S1 through S4 are turned on.

Mode4: output voltage of VO= -Vdc/4, upper switch S4 and three lower switches S5, S6 and S7 are turned on.

Mode5: output voltage of VO = -Vdc/2, all lower switches S5 through S6 are turned on.
The output voltage VO has five states: Vdc/2, Vdc/4, 0, - Vdc/4 and - Vdc/2. The gate signals for the chosen five level DCMLI are developed using MATLABSIMULINK.

Table 1 Switching Scheme for five Level DCMLI

S1	S2	S3	S4	S5	S6	S7	S8	Vo
1	1	1	1	0	0	0	0	Vdc/2
0	1	1	1	1	0	0	0	Vdc/4
0	0	1	1	1	1	0	0	0

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0	0	0	1	1	1	1	0	-Vdc/4
0	0	0	0	1	1	1	1	-Vdc/2

III. OPERATION OF THE PROPOSED CONVERTER

The proposed converter and its key waveforms are shown in Fig. 3 and 4. The proposed converter uses auxiliary windings that are taken from the converter transformer to act As "magnetic switches" to cancel the dc bus capacitor voltage so that the voltage that appears across the diode bridge output is zero. When the primary voltage of the main transformer is positive, Auxiliary Winding 1 cancels out the dc bus voltage so that the output voltage of Diode Bridge 1 (DB1) is zero and the currents in input inductors La1, Lb1, and Lc1 rise. When the primary voltage of the main transformer is negative, Auxiliary Winding 2 cancels out the dc bus voltage so that the output voltage of Diode Bridge 2 (DB2) is zero and the currents in input inductors La2, Lb2, and Lc2 rise. When there is no voltage across the main transformer primary winding, the total voltage across the dc bus capacitors appears at the output of the diode bridges and the input currents falls since this voltage is greater than the input voltage. If the input currents are discontinuous, then they will be naturally sinusoidal and in phase with the input voltages. The converters modes of operation are explained in this section. Typical converter waveforms are shown in Fig. 3. The equivalent circuit in each stage is shown in Fig. 4.The converter goes through the following modes of operation.

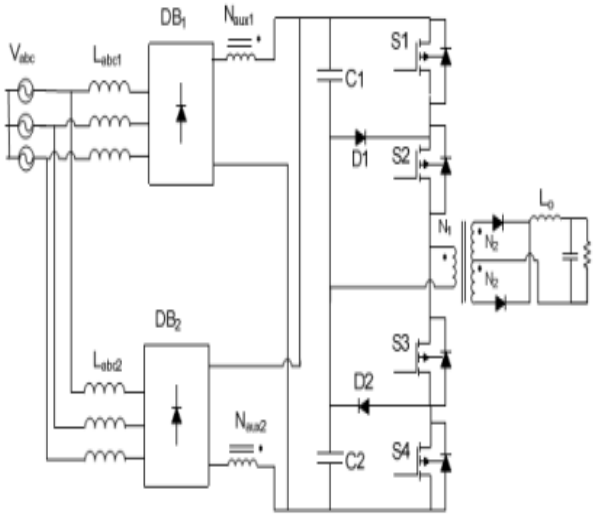

Fig.3. Proposed interleaved three-stage three-level converter.

Mode 1 (t0< t < t1) (Fig. 5):

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During this interval, switches S1and S2 are ON. In this mode, energy from dc bus capacitor C1flows to the output load. Due to magnetic coupling, a voltage appears across Auxiliary Winding 1 that cancels the total dc bus capacitor voltage; the voltage at the diode bridge output is zero and the input currents in La1, Lb1, and Lc1 rise.

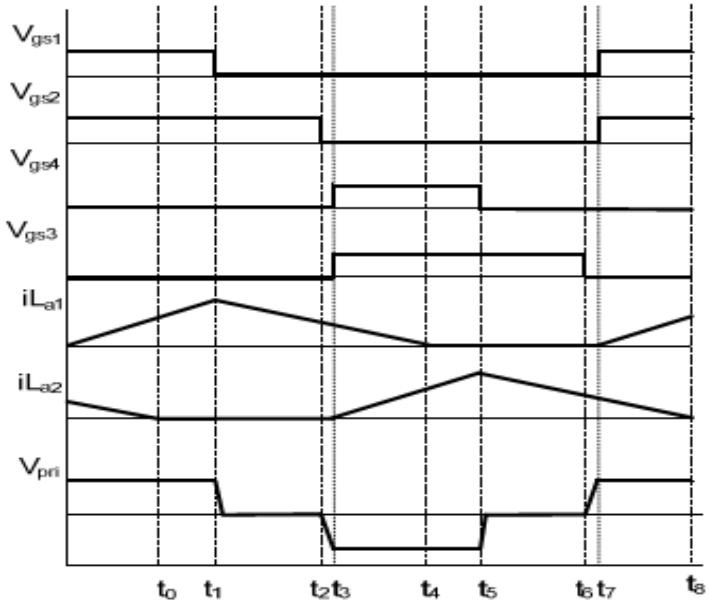

Fig. 4. Typical waveforms describing the modes of operation.

Mode 2 (t1< t < t2) (Fig. 6):

In this mode, S1 is OFF and S2 remains ON. The energy stored in L1during the previous mode starts to transfer into the dc bus capacitor. The primary current of the main transformer circulates through D1and S2. With respect to the converter's output section, the load inductor current freewheels in the secondary of the transformer, which defines a voltage across the load filter inductor equal to –VL.

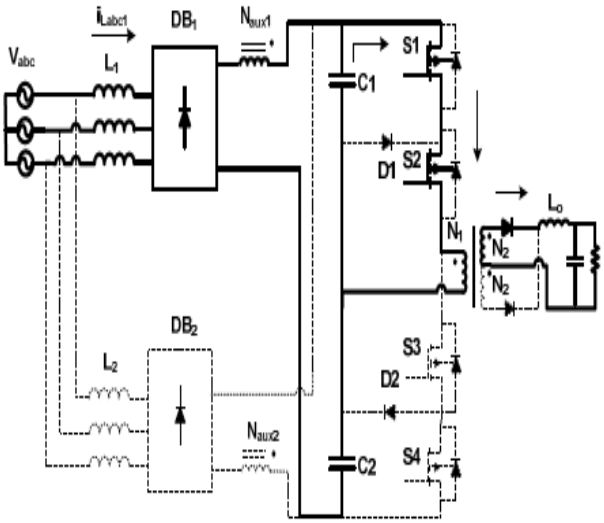

Fig.5. Mode 1 operation of interleaved three-stage three-level converter.

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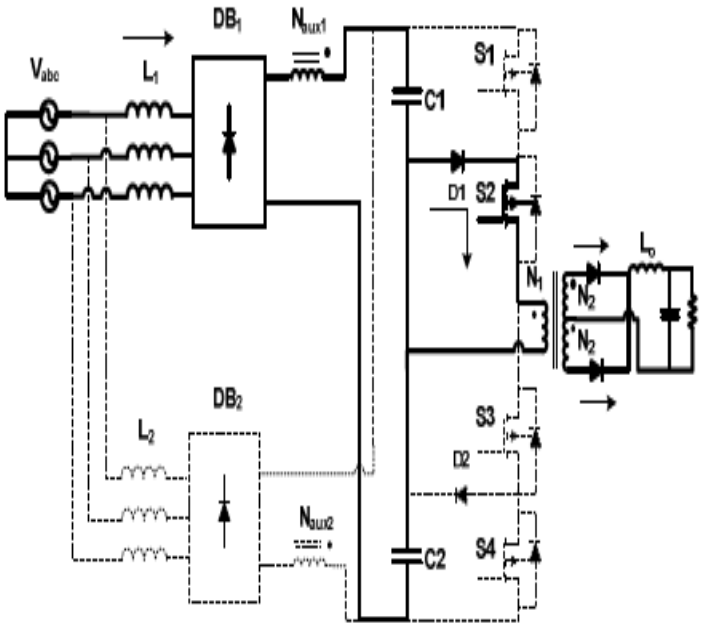

Fig.6. Mode 2operation of interleaved three-stage three-level converter.

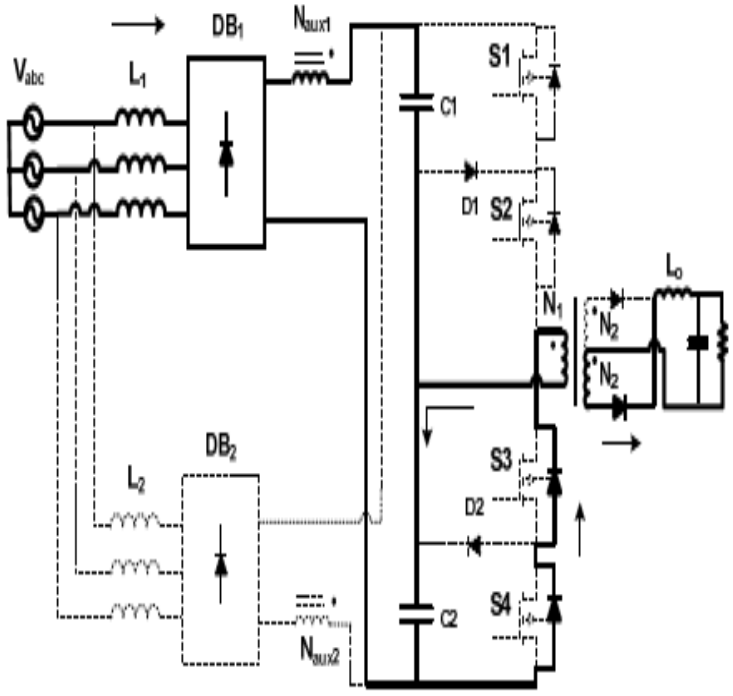

Fig.7. Mode 3 operation of interleaved three-stage three-level converter.

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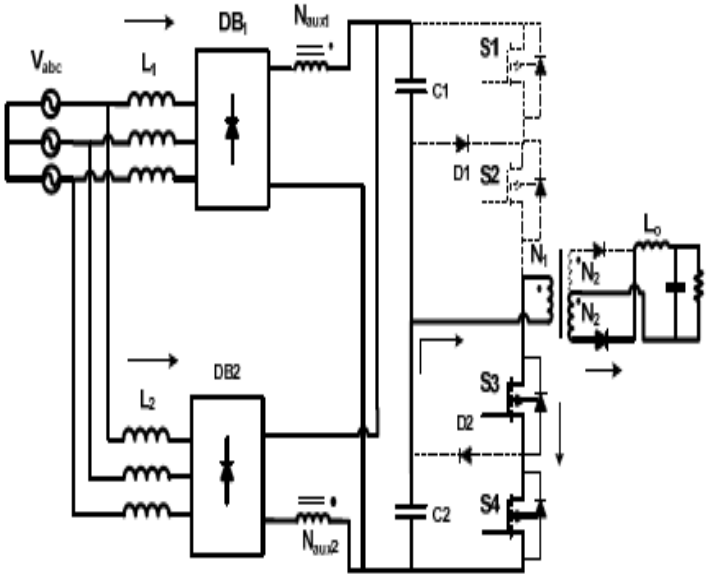

Fig.8. Mode 4 operation of interleaved three-stage three-level converter.

Mode 3 (t2< t < t3) (Fig. 7)

In this mode, S1and S2 is OFF. The energy stored in L1still is transferring into the dc bus capacitor. The primary current of the transformer charges C2 through the body diodes of S3and S4. Switches S3 and S4 are switched ON at the end of this mode.

Mode 4 (t3< t < t4) (Fig. 8)

In this mode, S3 and S4 are ON and energy flows from the capacitor C2 into the load. The magnetic switch cancels out the dc bus voltage and voltage across the auxiliary inductors L2 becomes only the rectified supply voltage of each phase and the current flowing through each inductor increases. This mode ends when the energy stored in L1completely transfers into the dc bus capacitor. For the remainder of the switching cycle, the converter goes through Modes 1 to 4, but with S3 and S4 ON instead of S1and S2and DB2instead of DB1.It should be noted that input current is summation of inductor currents iL1and iL2 which are both discontinuous. However, by selecting appropriate values for L1(= La1= Lb1= Lc1) and L2(= La2= Lb2= Lc2) in such a way that two inductor currents such as iLa1and iLa2have to overlap each other, the input current can be made continuous as shown in Fig. 9; thus reducing the size of input filter significantly. There is a natural 180^{o} phase difference between the currents in L1 and the currents in L2 as one set of currents rises when the transformer

$$i_{La} = i_{La1} + i_{La2}$$

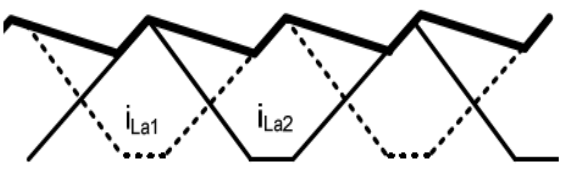

Fig.9. Interleaving between two input inductor currents.

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Primary is impressed with a positive voltage and the other set rises when the transformer primary is impressed with a negative voltage – these two events occurs 180^{o} apart during a switching cycle.

IV. MATLAB/SIMULINK RESULTS

Here simulation is carried out in several cases, in that, 1). Evaluation of Proposed Three Level AC-DC Converter under Power Factor Correction Mode 2). Evaluation of Proposed Five level AC-DC Converter under Power Factor Correction Mode.

Case 1: Evaluation of Proposed AC-DC Converter under Power Factor Correction Mode

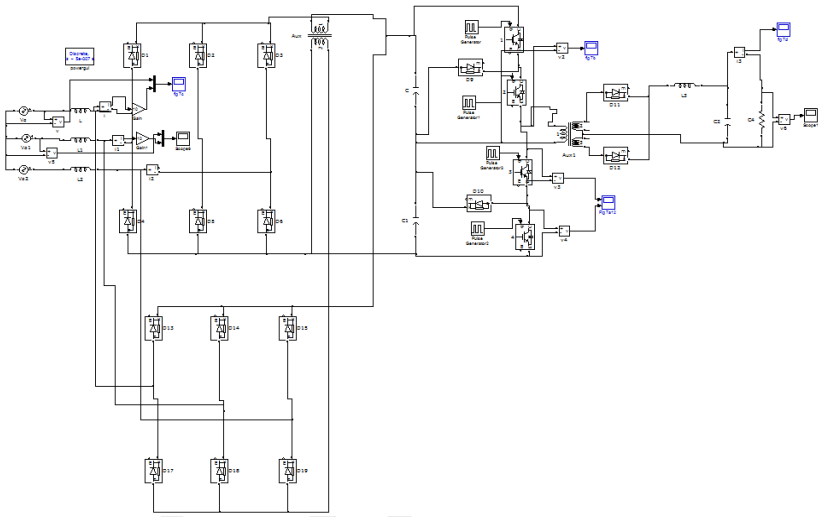
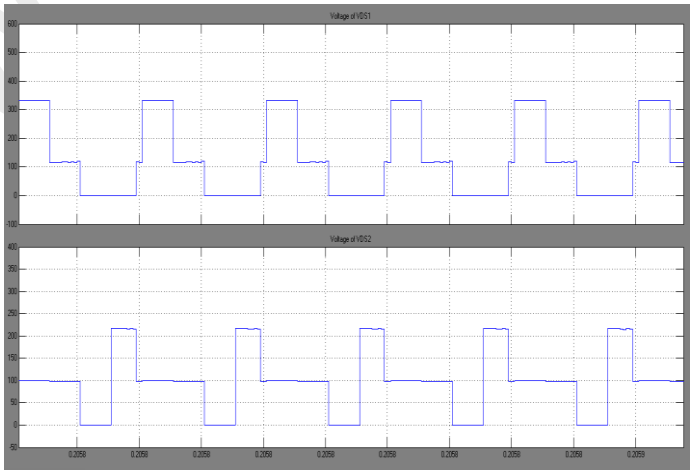


Fig.10. Matlab/Simulink Model of Proposed AC-DC Converter under Power Factor Correction Mode.

Fig.10. shows the Matlab/Simulink Model of Proposed AC-DC Converter under Power Factor Correction Mode using Matlab/Simulink Software package.



(a) Voltages of VDS1 & VDS2

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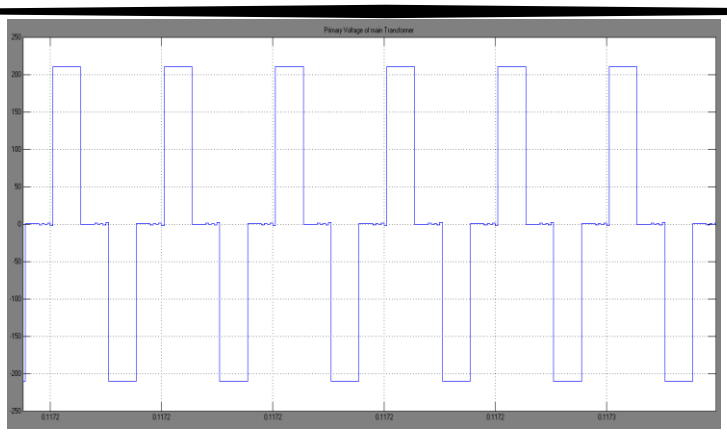
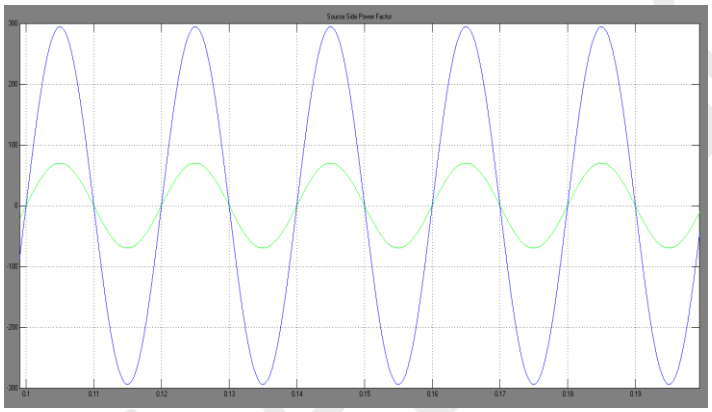
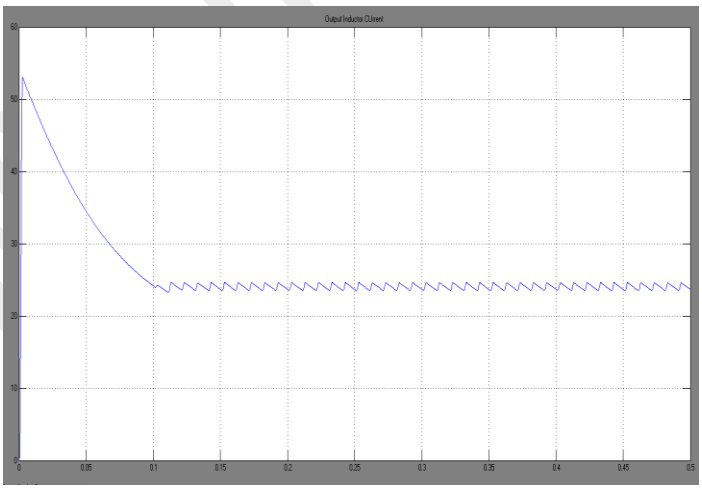


(b) Primary Voltage of Main Transformer



(c) Source Side Power Factor



(d) Output Inductor Current

Fig. 11 Simulation Results of Proposed AC-DC Converter under Power Factor Correction Mode, in that represents (a) Voltage at VDS1 & VDS2 Switches, (b) Primary Voltage of Main Transformer, (c) Source Side Power factor, (d) Output Inductor Current.

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Case 2: Evaluation of Proposed Five level AC-DC Converter under Power Factor Correction Mode

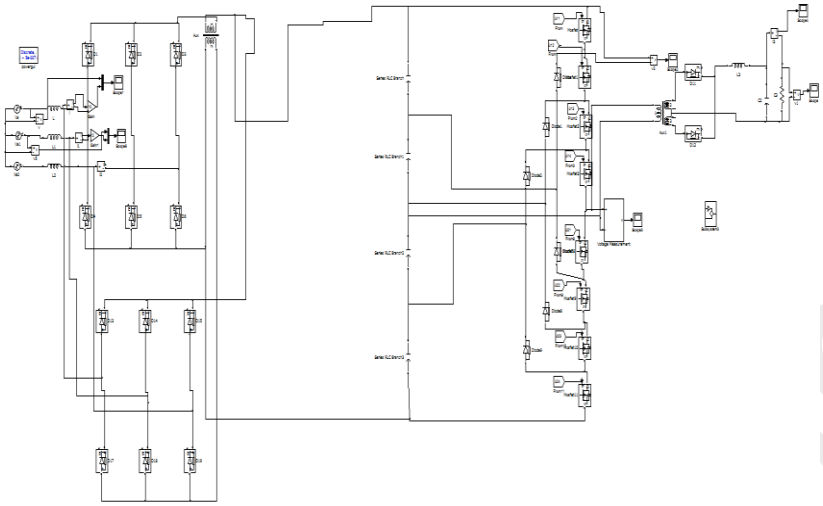
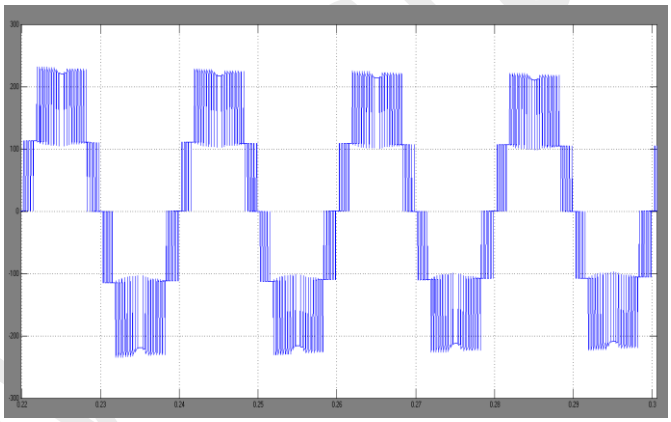
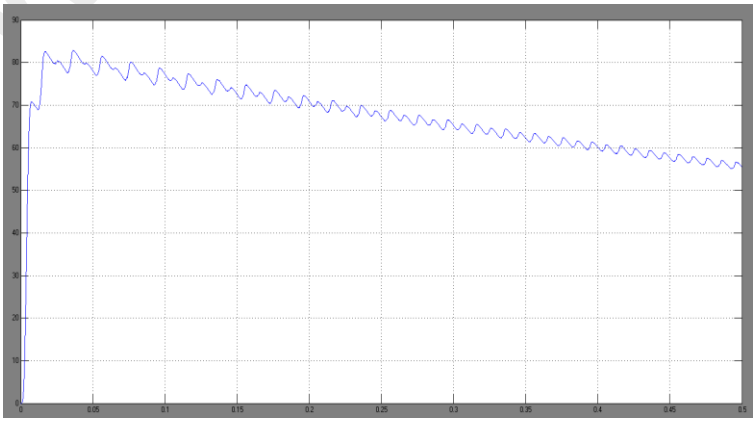


Fig.12 Matlab/Simulink Model of Proposed 5-Level AC-DC Converter under Power Factor Correction Mode.

Fig.12. shows the Matlab/Simulink Model of Proposed 5-Level AC-DC Converter under Power Factor Correction Mode using Matlab/Simulink Software package.



(a) Primary Voltage of main Transformer (Five Level Voltage)



(b) Output Voltage

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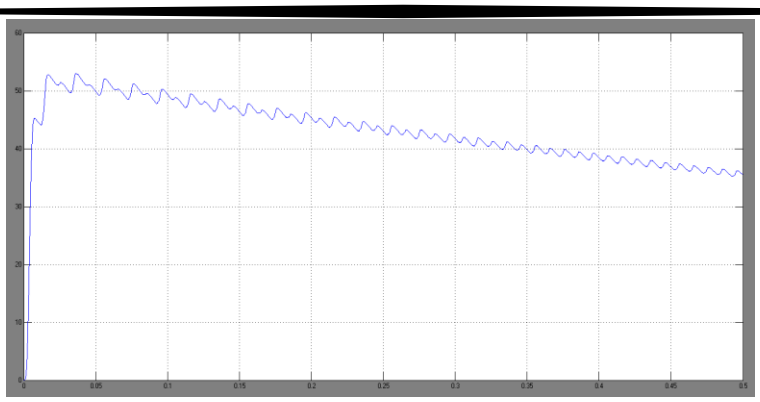
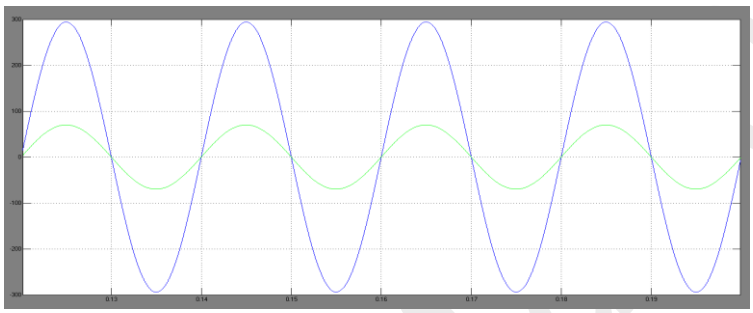


(c) **Output Current**



(c) Source Side Power Factor

(d)

Fig. 13 shows the Simulation Results of Proposed 5-Level AC-DC Converter under Power Factor Correction Mode, in that represents (a) Primary Voltage of Main Transformer, (b) Output Voltage (c) Output Inductor Current, (d) Source Side Power factor.

V.CONCLUSION

The proposed converter can operate with an input current harmonic content that meets the EN61000-3-2 Class Constructing new power converters that are suitable for medium to high voltage range applications is a great challenge for power electronics. The need for solid-state ac-dc converters to improve power quality in terms of power-factor correction (PFC), reduced total harmonic distortion at input ac mains, and precisely regulated dc output have motivated the proposal of several topologies based on classical converters. Here proposed a three-phase, three-level and five levels, single-stage power-factor corrected AC/DC converter that operates to regulate the output voltage was presented in this paper. The proposed converter has the following features. Proposed converter can operate with lower peak voltage stresses across the switches and the dc bus capacitors as it is a three-level & five level converters. This allows for greater flexibility in the design of the converter and ultimately improved performance.

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