

Design and VLSI Implementation of Oversampling Sigma Delta Digital to Analog Converter Used For Hearing Aid Application

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ABSTRACT:

Signal processing of present era is becoming more and more complex day by day. To meet the demand of modern signal processing, emphasis has been given to develop systems with minimum hardware. As a matter of fact, reduction in hardware complexity of digital filter has emerged as one of the upcoming research areas in present time. The most basic interpolation system for integer up sampling cascades an expander unit with an interpolation low pass filter. The low pass filter is used to remove the unwanted spectral images caused due to up sampling. The proposed system uses an half band elliptic IIR low pass filter implemented as a parallel connection of two all pass filter sections and sigma delta modulators to implement the Digital To Analog Converter(DAC). The filter coefficient implemented using only adders / shifters. The method described here is intended for quick design at the system level without the use of intensive calculation. The design aims to provide low computational hardware when compared to other filters.

Keywords—interpolator; elliptic filter; DAC

I. INTRODUCTION

Digital signal processing (DSP) refers to the technique of representing digital signal to improve accuracy and reliability of digital communication. Digital filters play very important roles in DSP systems. There are many applications in which the signal at a given sampling rate needs to be converted into another signal with different sampling rates. To change the sampling rate of the digital signal multi-rate systems use a down sampler and an up sampler in addition to other devices. But this rate conversion leads to production of undesired signals associated with aliasing and imaging errors. So some kind of filter has to be placed to attenuate these errors.

The growth of portable digital audio products has increased the demand for an audio digital to analog converter (DAC). The number of portable digital audio products is tremendously increasing in recent days the main concern is of these devices are their cost and power consumption. Interpolator is an integral part of digital audio DAC which is used to relax the design requirements for analog filters.

The recent trend in the design of audio interpolation filters is focused on the use of IIR based approaches. Multi-rate filters are the interpolation and decimation filters that increases or decreases the sampling rate of a signal respectively. Interpolation is the property of inserting

new sample values between existing samples. Interpolation rate change by an integer factor has been used in many modern digital communication systems.

A general block diagram for a sigma-delta DAC is depicted in Figure 1. It consists of four functionally different parts. In the first phase, the sampling rate of the input discrete-time signal is increased using an interpolation filter. In the second phase, the noise shaper converts an n-bit input data stream into a 1-bit data stream. This data stream is converted in the third phase into an analog signal using a 1-bit DAC.

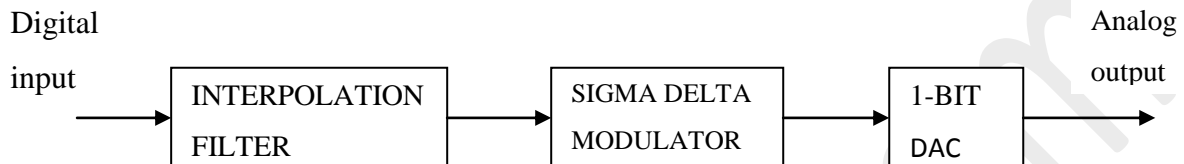


Fig:1 General block diagram of sigma delta DAC

Due to the oversampling nature of $\Sigma-\Delta$ modulators, an interpolation filter is needed prior to the modulator. The interpolation filter can be modelled as either FIR or IIR filters. The primary advantage of FIR based interpolation filters is their linear phase response. But in order to meet the stringent filtering requirements their complexity increases sharply. Increasing the order of FIR based interpolators not only increases the hardware complexity but also the group delay of the filter which cannot be tolerated in the live audio applications. For such applications, IIR filters seem to be more attractive option. IIR filters are computationally more efficient, which allows greater processing flexibility compared to an FIR filter.

The proposed work includes the implementation of a oversampling digital to analog convertor used for the hearing aid application using sigma delta modulator. This work aims to reduce the hardware demand.

II. INTERPOLATION

Interpolation is a process of increasing the sampling rate and the system which performs it is called interpolator. The aim of the interpolation is to get a new sequence with higher sampling rate without losing the information. Interpolation is a two-stage process, first the input signal is upsampled and then the upsampled signal is filtered. In the first stage, L-1 zero-valued samples are inserted in between consecutive samples of the original sequence, where L is the interpolation factor. Fig.2 shows the general block diagram of the interpolation filter.

The signal generated after the upsampling is given by,

$$x_u[n] = \begin{cases} \frac{x}{L} & n = 0, \pm L, \pm 2L \\ 0 & \text{otherwise} \end{cases}$$

Where L is the sampling rate of the signal.

The up sampled signal consists of some additional images this image has to be removed so an anti-imaging filter is used at the output of the interpolator. The anti-imaging filter is a low pass filter, when the value of $L=2$ the filter can be implemented as a half band filter. This filters reduce the bandwidth of a signal roughly by half and are suitable for decimation/interpolation by a factor of 2. Nyquist filters are characterized by the fact that every L^{th} sample of its impulse response (i.e. every L^{th} filter coefficient) is equal to zero. In the case of half band filters this fact is particularly appealing since it means that roughly half of its coefficients are equal to zero. This of course makes them very efficient to implement. As such, half band filters are widely used in particular for multi-rate applications including multistage applications. The cutoff frequency for a half band filter is always 0.5π . Moreover, the pass band and stop band ripples are identical, limiting the degrees of freedom in the design.

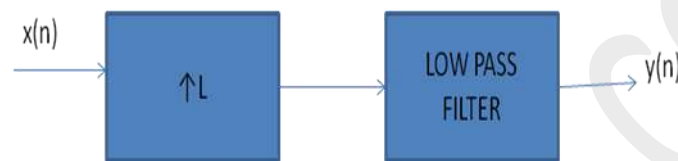


Fig.2 General block diagram of interpolation filter

III FILTER DESIGN

An odd order bounded real IIR low pass transfer function with symmetric numerator and no common factors with its numerator and denominator, can be decomposed into a sum of two stable all pass filter functions provided its power complementary high pass IIR transfer function has an asymmetric numerator and satisfying the condition,

$$H(z)H(z^{-1}) + H(-z)H(-z^{-1}) = 1 \quad (1)$$

The sum of all pass decomposition is of the form

$$H(z) = \frac{1}{2} [A_0(z^2) + z^{-1}A_1(z^2)] \quad (2)$$

Where $A_0(z)$ and $A_1(z)$ are stable all pass filter sections. Since the pass band and stop band ripples of the chebyshev IIR filter are not equal, it is not possible to design a chebyshev IIR half band filter. Therefore only butterworth and elliptic half band filters can be designed. Any odd order elliptic lowpass half band filter $H(z)$ with a frequency response specification given by

$$\begin{aligned} 1 - \delta_p &\leq |H(e^{j\omega})| \leq 1, & \text{for } 0 \leq \omega \leq \omega_p & \quad (3) \\ |H(e^{j\omega})| &\leq \delta_s, & \text{for } \omega_s \leq \omega \leq \pi & \end{aligned}$$

and satisfying the condition,

$$\omega_p + \omega_s = \pi \quad (4)$$

$$\delta_s^2 = 4\delta_p(1 - \delta_p) \quad (5)$$

is a power-symmetric transfer function and can always be expressed as in Eq.(2). Since the two bandedges are related through Eq.(4) and the two ripples are related through Eq. (5), the filter specifications include only one of the bandedges and one of the ripples. The specified pass band edge and stopband ripple be ω_p and δ_s respectively. The pass band edge ω_p and the pass band ripple δ_s are then determined from Eq.(4) and (5). The minimum stopband attenuation is therefore $A_s = -20 \log_{10} \delta_s$ dB, and the maximum pass band ripple is $A_{max} = -20 \log_{10}(1 - 2\delta_p)$ dB [7]. The selectivity factor k is calculated as $k = \omega_p / \omega_s$. Using the selectivity factor the modular constant q is calculated as follows:

$$q = u + 2u^5 + 15u^9 + 150u^{13} \quad (6)$$

where the value of u is given by,

$$u = \frac{1 - \sqrt[4]{1 - k^2}}{2(1 + \sqrt[4]{1 - k^2})}$$

Using the values of A_p and A_s the discrimination factor D is calculated as

$$D = \frac{10^{A_s/10} - 1}{10^{A_p/10} - 1} \quad (7)$$

The minimum required order of the filter is calculated by

$$n = \left\lceil \frac{\log 16D}{\log\left(\frac{1}{q}\right)} \right\rceil \quad (8)$$

Where, $\lceil x \rceil$ denotes the smallest integer equal to or greater than x .

The co-efficient of the elliptic filter, can be computed as follows.

$$\lambda_k = \frac{2q^{1/4} \sum_{i=0}^{\infty} (-1)^i q^{i(i+1) \sin((2i+1)k\pi/N)}}{1 + 2 \sum_{i=0}^{\infty} (-1)^i q^{i^2} \cos(2\pi ki/N)} \quad (9)$$

$$b_k = \sqrt{(1 - r\lambda_k^2) \left(1 - \frac{\lambda_k^2}{r}\right)} \quad (10)$$

$$c_k = \frac{2b_k}{1 + \lambda_k^2} \quad (11)$$

and

$$a_{k-1} = \frac{2-c_k}{2+c_k} \quad (12)$$

The filter transfer function is obtained using the above equations.

IV SIGMA DELTA MODULATOR

Delta-sigma modulators are often used in digital to analog converters (DACs). In general, a DAC converts a digital number representing some analog value into that analog value. For example, the analog voltage level into a speaker may be represented as a 20 bit digital number, and the DAC converts that number into the desired voltage. To actually drive a load (like a speaker) a DAC is usually connected to or integrated with an electronic amplifier.

In case, a multi-bit digital number is input to the delta-sigma modulator, which converts it into a faster sequence of 0s and 1s. These 0s and 1s are then converted into analog voltages. The conversion, usually with MOSFET drivers, is very efficient in terms of power because the drivers are usually either fully on or fully off, and in these states have low power loss.

The resulting two-level signal is now like the desired signal, but with higher frequency components to change the signal so that it only has two levels. These added frequency components arise from the quantization error of the delta-sigma modulator, but can be filtered away by a simple low-pass filter. The result is a reproduction of the original, desired analog signal from the digital values.

The use of a delta-sigma modulator in the digital to analog conversion has enabled a cost-effective, low power, and high performance solution.

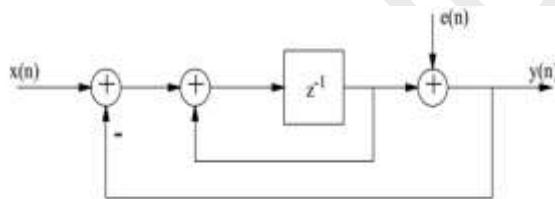


Fig.3 First order $\Sigma\Delta$ modulator

The above block diagram represents a first order sigma delta modulator. As depicted in fig.3, output signal is fed back and subtracted from the input of the modulator. The model for the signal feedback consists of an input signal $x(n)$, $e(n)$ defines the quantization bits and $y(n)$ is the output of the modulator. The transfer function of the first order sigma delta modulator is given by,

$$Y(z) = Y(z) = X(z)z^{-1} + e_Q(1 - z^{-1}). \quad (13)$$

An integrator as shown in fig.2, consists of an adder and a delay element, is a part of signal feedback model. The adder accumulates delayed output with the next input of the sigma-delta modulator. The next component which is a part of the first-order sigma-delta modulator is a quantizer. In the model of sigma-delta modulator we assume that the quantization

noise is not correlated with the input signal. The quantizer can be modeled as a block that has a linear gain and independent noise source which adds quantization noise. The last part of sigma-delta modulator is a feedback loop. Sigma-delta modulators modify the spectral properties of the quantization noise, in such a way that the quantization noise is low in the band of interest. The modulator also tries to move or shape the noise contents to higher frequencies, and this noise shaping is achieved with the help of a negative feedback loop.

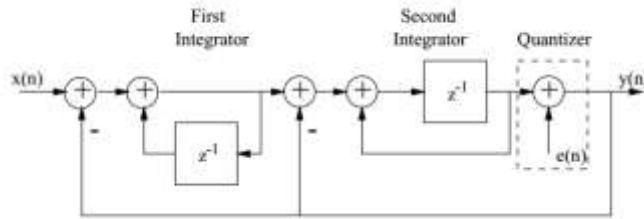


Fig.4 Second order sigma delta modulator

Fig.4 shows a second-order signal feedback model, in which two first-order signal feedback models are cascaded. The transfer function for second-order signal feedback model is given by

$$Y(z) = X(z)z^{-1} + E(z)(1 - z^{-1})^2. \quad (14)$$

V SIMULATION RESULTS

The IIR half band interpolator is simulated in Modelsim, version Modelsim.SE 6.4a software which shows the filter input and output value. Hearing aids normally have a bandwidth of $BW=10\text{kHz}$. To fulfill the Nyquist criterion, the input sampling frequency in this example is half of the standard high-fidelity audio sampling frequency $f_{s,in} = 44.1\text{kHz}/2 = 22.05\text{kHz}$. The interpolation factor is two; therefore, the output sampling frequency is $f_{s,out} = 44.1\text{kHz}$. Thus, the normalized pass band cutoff frequency is $\omega_p = (2\pi \times 2 \times 10\text{kHz}) / (2\pi \times 44.1\text{kHz}) = 0.4535$. Due to the symmetry of the half-band filter, $\omega_s = 1 - \omega_p = 0.5465$, and the normalized transition band is $\omega_t = \omega_p - \omega_s = 0.093$. The filter is designed for the specification with the pass band ripple of 0.01dB and stop band attenuation of 60dB. The coefficient of the filter are obtained using the Eq.(9,10,11,12). The Fig.5 shows the simulation results for IIR elliptic interpolator and the Fig.6 shows the results obtained for sigma delta modulation. The comparison results for the above is shown in table 1. It can be noted that the digital to analog convertor using the butterworth filter has the highest number of slices, flip flops and 4 input LUT used, compared to that of digital to analog convertor using elliptical filter. As the elliptical filter can be analyzed within a minimum order for the same specified frequency as the butterworth filter requires minimum hardware components. The Fig.7 shows the graphical representation of the hardware requirements of the interpolation filter. It can be observed that the bar drawn for DAC using butterworth filter uses the number of slices, number of slices flip flop, number of 4 input LUT nearly equal to 1274, 131, 2416 and for DAC using elliptical filter as 293, 128, 537 respectively. From the experimental results it can be concluded that the Digital to Analog convertor using elliptical filter has minimum area.

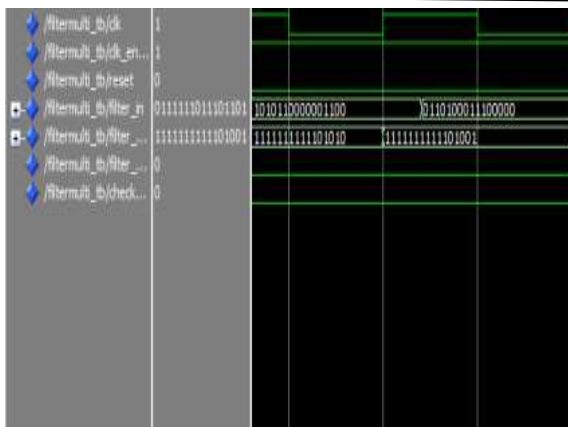


Fig.5 Simulation result for IIR elliptic

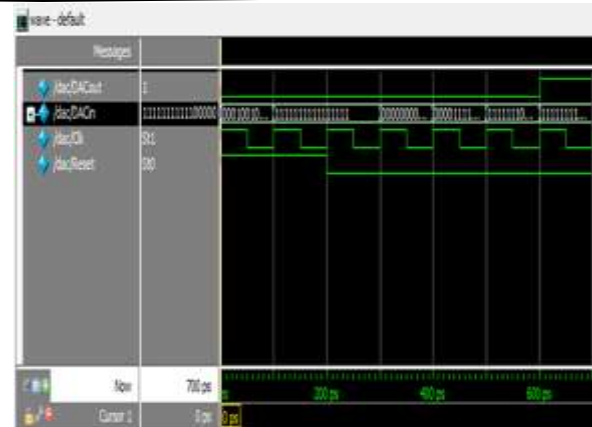


Fig. 6 Simulation results for Sigma delta modulator

Interpolation filter.

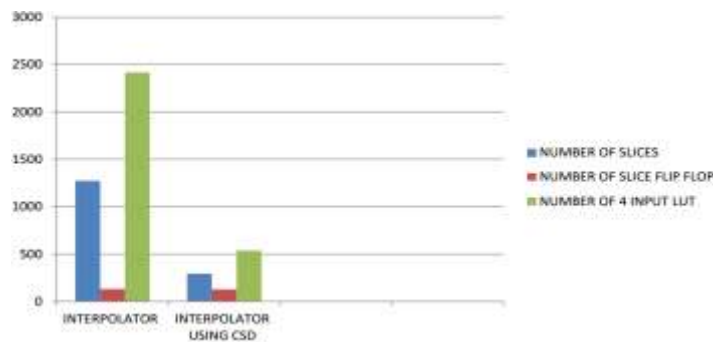


Fig.7 Graphical representation of the comparison.

Hardware Component	DAC using butterworth filter	DAC using elliptic filter
Number of slices	1274/3584	293/3584
Number of slices flip flop	131/7168	128/7168
Number of 4 input LUT's	2416/7168	537/7168

VI CONCLUSION

The proposed sigma delta modulator based oversampled digital to analog converter is a very effective way for low power, high resolution convertors which can be ultimately integrated on digital signal processor ICs. Here a second order delta sigma delta modulator is used as it reduces the quantisation noise. From the output obtained it is determined that the digital to analog convertor using IIR elliptical filter is found to be with minimum area.

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